Simple Tracker™ with Power-Good Comparator

Preliminary Technical Data

ADM1202

FEATURES

- Enables Power Supply Tracking of multiple supplies
- Up/Down Tracking limits Supply Differences to ~100mV
- Capacitor Adjustable Slew Rate
- On Board Charge Pump Fully enhances FET
- Ability to Track Down Supplies (ADM1202-1)
- Emergency Shutdown Feature (ADM1202-2)
- In-Built Power Good Detector Circuitry
- Packaged in tiny 8-Lead TSOT Package

APPLICATIONS

- Multi-Voltage Supply Rail Tracker
- Telecoms and Datacom s Systems
- Multi voltage Network Processors , FPGAs, ASICs, DSPs
- PC/Server Applications

GENERAL DESCRIPTION

The ADM1202 is a cascadable Simple Tracker ™ device which ensures that voltage rails track within ~100mV of each other in multi supply systems. Any number of these devices can be cascaded to form a multi supply tracking solution.

The ADM1202 requires 2.7V to 16.5V on its Vcc pin to operate. An on-board charge pump generates a high voltage GATE drive to fully enhance FETs in the power path.

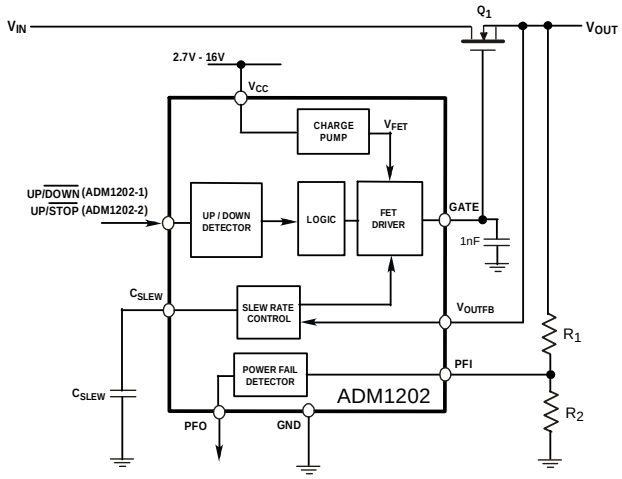
The Slew Rate of the ramp is adjustable via an external capacitor on the C_{SLEW} pin and can be programmed from 100V/s to 1000V/s. When multiple devices are cascaded the C_{SLEW} pin of each subsequent device should be tied to the output rail(V_{OUTFB}) of the previous device to ensure that supply will track up and down with the previous supply.

The ADM1202 is offered in two variants. The ADM1202-1 features an UP/DOWNb pin and the ADM1202-2 features an Up/STOPb pin. For both devices a high level on the this input will initiate tracking power up sequence. A low on the UP/DOWNb pin of the ADM1202-1 will initiate a tracking down of the supply rails, while a low on the UP/STOPb pin of the ADM1202-2 will initiate an emergency fast shutdown of all supply rails simultaneously.

Power Fail Detector circuitry is also present. A resistor divider on the PFI input will dictate what level the ADM1202 registers a power fail on that supply. When a power fail is detected the Power Fail Output (PFO) will assert.

The ADM1202 is packaged in a tiny 8-pin TSOT package.

Functional Block Diagram



Applications Diagram

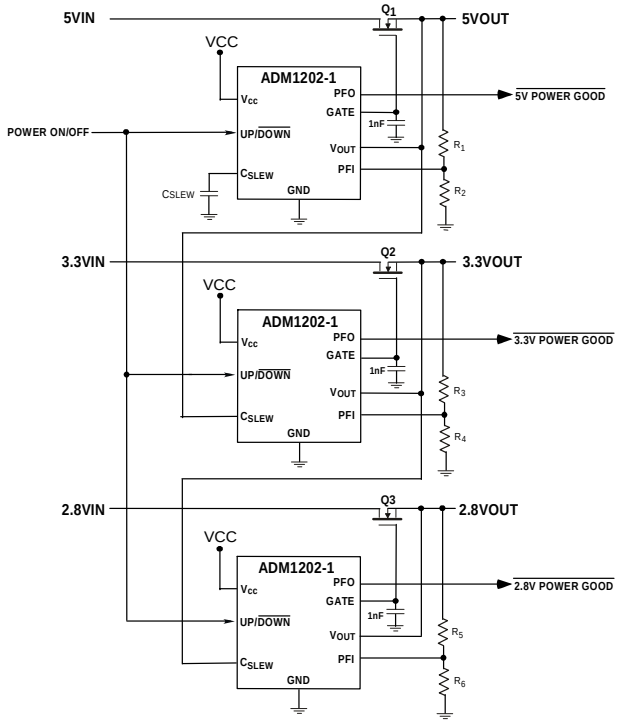


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Table 1. V_{CC} = Full Operating Range, T_A = -40°C to +85°C, unless otherwise noted.

Parameter	Min	Typ	Max	Units	Conditions
V_{CC} Pin					
Operating Voltage Range Vcc	2.7		16.5	V	
Undervoltage Lockout, V_{UVLO}	2.4	2.525	2.65	V	Vcc Rising
UVLO Hysteresis		25		mV	
Switched Voltage Range	0.65		16.5	V	
Quiesent Current		0.65	1.0	mA	
Up/Downb Pin					
Input Threshold	0.58	0.6	0.62	V	Rising
Input Threshold Hysteresis		60		mV	
Input Current	-100		100	nA	
Power Fail Output, PFO Pin					
Internal Pull Up		-5		µA	
Output Low Voltage			0.4	V	Note 1, Iload = 300uA
Power Fail Detector, PFI Pin					
PFI Detector Threshold	0.58	0.6	0.62	V	
PFI Detector Hysterisis		10		mV	
PFI Input Current	-100		100	nA	
C_{SLEW} Pin					
Slew up Current		-10		µA	
Slew down Current		10		µA	
Tracking Gain		1		V/V	V_{SLEW}/V_{OUTFB}
Minimum Tracking Voltage		0.1		V	
Maximum Tracking voltage		Vcc – 0.3		V	
Slew Rate	100		1000	V/s	
V_{OUTFB} Pin					
Input Current	-10		10	µA	
Voltage Range	0		Vcc	V	
GATE Pin					
Gate Pullup Current		12		µA	Vslew – Vout > 100mV
Gate Pulldown Current		12		µA	Vout – Vslew > 100mV
Gate Pulldown Current		2		mA	ADM1202-2 only –vgate = 3.0V
GATE Voltage, V_{GATE}	5	6.5	10	V	$V_{GATE} – V_{CC}$; V_{CC} = 2.7V
	6	8	12	V	$V_{GATE} – V_{CC}$; V_{CC} = 5.0V
	5	6.5	10	V	$V_{GATE} – V_{CC}$; V_{CC} = 16.5V

NOTES:
[1] Asserted when voltage on PFI pin exceeds threshold

Absolute Maximum Ratings

Table 2. ADM1202 Absolute Maximum Ratings

Parameter	**Rating**
V_{CC} Pin	20V
PFI Pin	20V
UP/DOWNb, UP/STOPb	20V
PFO Pin	20V
C_{SLEW} Pin	20V
Gate Pin	Vcc + 11V
V_{OUTFB} Pin	20V
Power Dissipation	TBD
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

ENABLING A SINGLE SUPPLY

The ADM1202 requires a supply voltage of 2.7V to 16.5V on its Vcc pin for operation. The device may be powered from the input supply rail that is being switched or from an auxiliary supply.

An internal charge pump ensures that the ADM1202 is capable of fully enhancing an external FET via the GATE pin, turning on the output. An external capacitor may be required on the GATE node for stability.

Power up can be externally initiated by driving the UP/DOWNb (ADM1202-1) or UP/STOPb (ADM1202–2) logic pin high. A low on this pin will initiate a power down.

The V_{OUTFB} pin monitors the output voltage.

A single ADM1202 device may be used where a single supply rail is required to switch on at a controlled slew rate (see Figure 1). The value of the slew rate capacitor, C_{SLEW}, will dictate the slew rate of the GATE voltage at startup. An internal current 10µA source charges C_{SLEW} and the GATE voltage is ramped at the same rate.

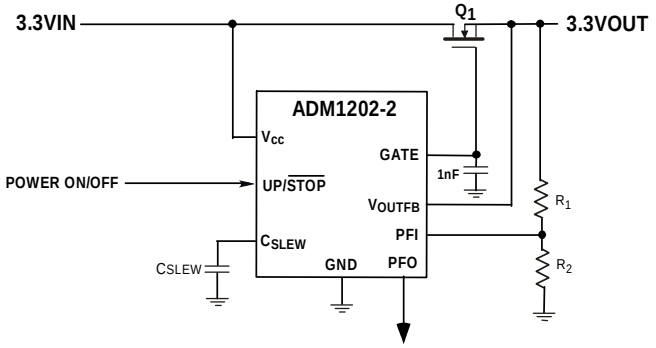


Figure 1. ADM1202 Switching on a Single Supply

MULTI-SUPPLY TRACKING

The primary function of the ADM1202 is to provide a voltage tracking solution for multiple supply rails. The implementation in Figure 2 will provide this function. Each voltage rail has its own ADM1202 device driving a FET.

The UP/DOWNb (ADM1202-1) or UP/STOPb (ADM1202-2) pins of all devices can be driven by a single logic input which will initiate a system power-up going high or power-down going low.

In figure 2, the ADM1202 is configured to control the ramp of the largest supply first. The output of the first device is connected to the slew pin on the second device to allow the rate of the first supply to control the rate of the second and so on.

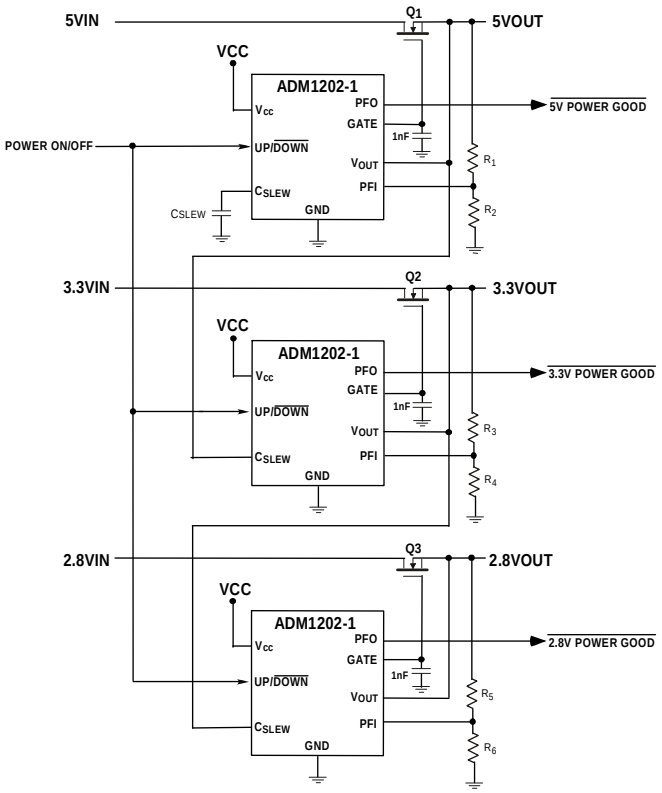


Figure 2. ADM1202 Solution for Tracking 3 Supplies

A low-to-high transition on the UP/DOWNb or UP/STOPb pin will initiate turn-on of the supplies. The ADM1202 will begin to source current into the C_{SLEW} capacitor. The voltages on all GATE pins will begin to rise, or "track" up, at the same rate, as set by the value of C_{SLEW}. All supply voltages will remain within 100mV of the C_{SLEW} voltage until they level off at their full potentials.

A high-to-low on the UP/DOWNb pin of the ADM1202-1 will initiate a tracking down of the supply rails. The voltages will attempt to stay with ~100mV of each other assuming the load current will be sufficient to discharge the capacitors at the required rate. (See Figure 3.)

A high-to-low on the UP/STOPb pin of the ADM1202-2 will initiate an emergency fast shutdown of all supply rails simultaneously. (See Figure 4.) Note that while the pass FETs will be turned off immediately the actual discharge rate of each supply rail will depend on the load.

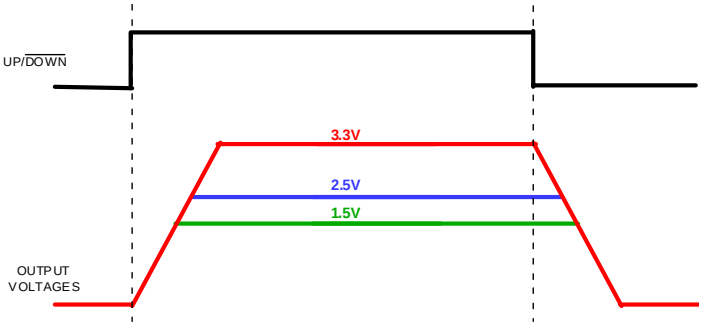


Figure 3. ADM1202-1 Power-Up and Power-Down Waveforms

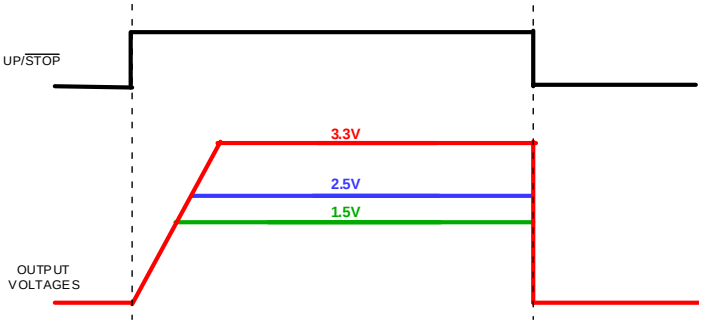


Figure 4. ADM1202-2 Power-Up and Power-Down Waveforms

ADM1202 POWER FAIL DETECTOR

Figure 4 shows the internal circuitry that enables the Power Fail Detector on the ADM1202. An internal comparator with a 0.6V reference is used for detection. An external resistor divider can be used to divide down a voltage rail to trigger a power fail fault at the appropriate level. The Power Fail Output, PFO, will assert high when a power fail condition occurs. Note that there is no internal shutdown action from a Power Fail event. A 10K is recommended on the PFO pin in order to ensure it is either pulled up or down during powerup. The pin will be in high impedance while Vcc < UVLO and may result in invalid power fail signals.

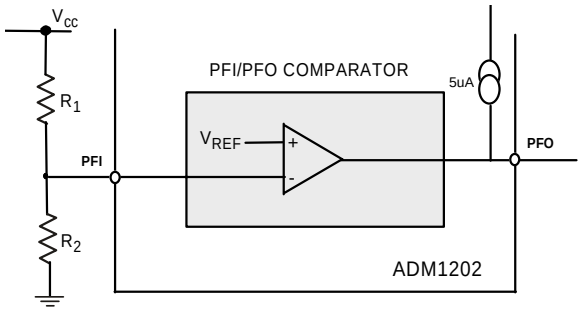


Figure 5. ADM1202 Internal Power Fail Detector circuitry

SLEW RATE CONTROL

Voltage tracking is achieved by controlling the slew rate of a rising or falling supply by an external capacitor on the SLEW pin. Alternatively, this pin can be overdriven with a supply which will result in the output following this supply. The gate responds to maintain ~100mV between the VOUTFB pin and the SLEW pin

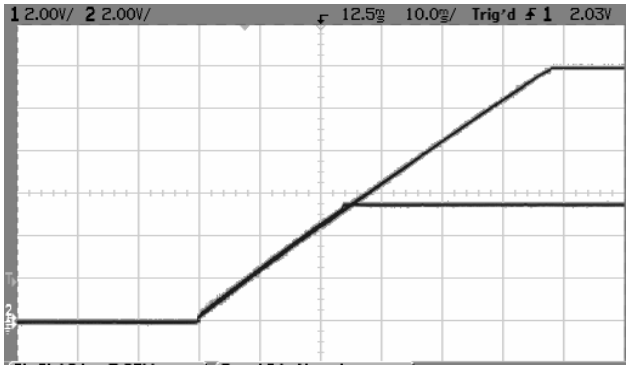
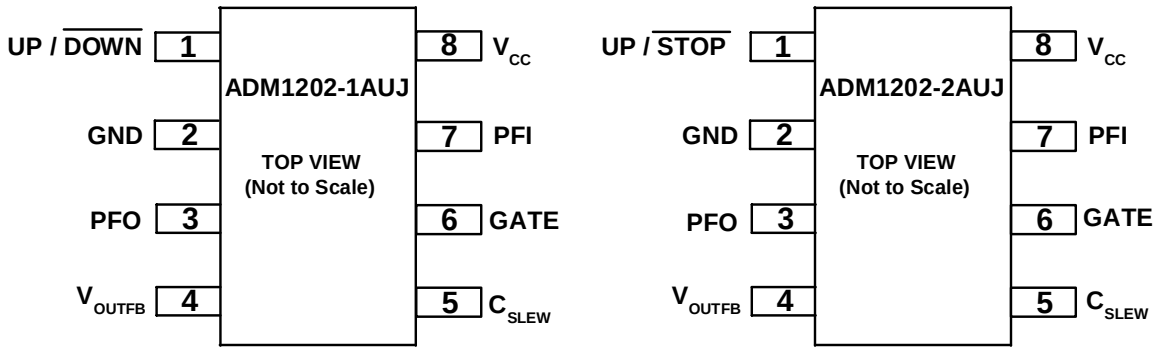


Figure 6. Tracking up Waveforms

PIN CONFIGURATIONS



PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Name	Description
1	UP/DOWNb or UP/STOPb	Logic Pin. Drive high to initiate track up off all ADM1202 controlled rails. Drive low to initiate track down of output (ADM1202-1) or a fast shutdown of output (ADM1202-2).
2	GND	Chip Ground Pin.
3	PFO	Logic Output. Asserts high when a power fail event occurs.
4	VOUTFB	Monitors the Source of the external FET
5	CSLEW	Connect to an external capacitor to control the slew rate of the output at turn on (and turn-off for ADM1202-1).
6	GATE	Drives the GATE node of the external FET
7	PFI	Power Fail Detector Input Pin. A power fail fault is registered at a voltage of 0.6V rising on this pin. An external resistor divider sets the output voltage that trips a power fail fault.
8	VCC	Chip Power Supply, 2.7V to 16.5V.

OUTLINE DIMENSIONS

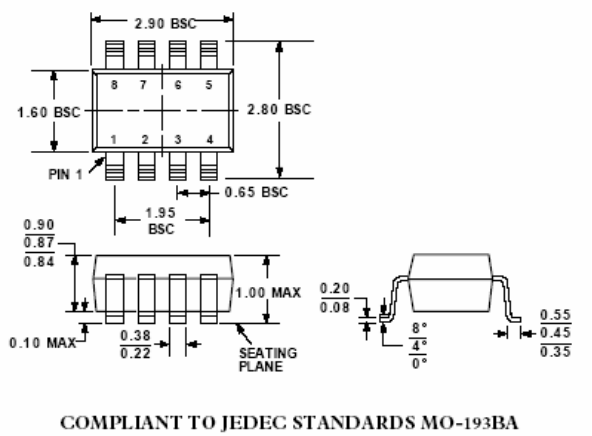


Figure XX. 8-Lead TSOT Package (UJ-8)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 3. Ordering Guide

Part Number	Variant	Temperature Package	Package Description	Package Outline
ADM1202-1AUJ	UP/DOWNb logic input	–40°C to +85°C	TSOT	UJ-8
ADM1202-2AUJ	UP/STOPb logic input	–40°C to +85°C	TSOT	UJ-8

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